Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-16. (Cancelled)

17. (Previously Presented) An integrated circuit formed from an etched organic low-k dielectric layer over a substrate, made from the steps comprising:

placing a hard mask over the organic low-k dielectric layer;

placing a patterned photoresist layer over the hard mask layer;

placing the substrate in an etching chamber;

providing an etchant gas comprising NH3 into the etching chamber;

generating a plasma from the NH3, which etches the organic dielectric layer, which is able to selectively etch the organic low-k dielectric layer with respect to the hard mask and strip the photoresist layer;

selectively etching the organic low-k dielectric layer with respect to the hard mask; and

simultaneously stripping the photo resist layer during the selective etching of the organic low-k dielectric layer.

18. (Previously Presented) The integrated circuit, as recited in claim 17, wherein the NH3 has a flow rate between 100 sccm to 1000 sccm.

19. (Canceled)

20. (Previously Presented) The integrated circuit, as recited in claim 17, wherein the NH3 has a flow rate from about 300 sccm to about 800 sccm.

21. (Previously Presented) The integrated circuit, as recited in claim 20, further comprising maintaining the substrate at a temperature between about 10° C to about 40° C during etching of the organic dielectric layer.

22. (Previously Presented) The integrated circuit, as recited in claim 17, further comprising providing a bias power of between about 0 W and 100 W during etching of the organic low-k dielectric layer.

23. (Previously Presented) The integrated circuit, as recited in claim 17, further comprising:

placing an etch stop layer over the organic low-k dielectric layer;

placing a second organic low-k dielectric layer over the etch stop layer, wherein the second organic low-k dielectric layer is between the organic low-k dielectric layer and the hardmask.

24. (Previously Presented) The integrated circuit, as recited in claim 23, further comprising etching the second organic low-k dielectric layer with a first etch, wherein the first etch provides a bias power of between about 250 W to about 2500 W before selectively etching the organic low-k dielectric layer.

25. (Previously Presented) The integrated circuit, as recited in claim 24, further comprising providing a bias power of between about 0 W and 100 W during etching of the organic dielectric layer.

26. (Previously Presented) The integrated circuit, as recited in claim 25, further comprising providing an etchant gas comprising CF4 for the etching the second low-k organic dielectric layer.

27. (Previously Presented) The integrated circuit, as recited in claim 26, wherein the etchant gas comprising CF4 further comprises C4F8.

28. (Previously Presented) The integrated circuit, as recited in claim 27, wherein the etchant gas comprising NH3 uses NH3 alone as the etchant.

29. (Previously Presented) The integrated circuit, as recited in claim 17, wherein the simultaneous stripping completely strips the photoresist.

30. (Previously Presented) The integrated circuit, as recited in claim 17, wherein the etchant gas comprising NH3 uses NH3 alone as the etchant.

31. (Previously Presented) An integrated circuit formed by a method of etching an organic dielectric layer over a substrate, comprising:

placing a hard mask over the organic dielectric layer;

placing a patterned photoresist layer over the hard mask layer;

placing the substrate in an etching chamber;

providing an etchant gas comprising NH3 into the etching chamber, wherein the NH3 has a flow rate between 5 sccm to 1500 sccm;

generating a plasma from the NH3, which selectively etches the organic dielectric layer with respect to the hardmask; and

simultaneously stripping the photo resist layer during the etching of the organic dielectric layer.

32. (Previously Presented) The integrated circuit, as recited in claim 31, further comprising providing CH3F while providing the etchant gas comprising NH3.

33. (Previously Presented) The integrated circuit, as recited in claim 32, further comprising providing an etch with an etchant gas comprising CF4, prior to the step of providing the etchant gas comprising NH3.

34. (Previously Presented) The integrated circuit, as recited in claim 33, wherein the etchant gas comprising CF4, further comprises C4F8.

35. (Previously Presented) The integrated circuit, as recited in claim 34, wherein the etchant gas comprising CF4 further comprises O2.

36. (Previously Presented) The integrated circuit, as recited in claim 31, wherein the organic dielectric layer is made of an organic low-k material, and wherein the simultaneous stripping completely strips the photoresist layer.

37. (Previously Presented) An integrated circuit formed by a method of etching an organic dielectric layer disposed below a hardmask layer and over a substrate, comprising:

placing the substrate in an etching chamber;

providing an etchant gas comprising NH3 into the etching chamber with a flow rate from about 300 sccm to about 800 sccm;

generating a plasma from the NH3, which etches the organic dielectric layer; and

maintaining the substrate at a temperature between about 10° C to about 40° C during the etching of the organic dielectric layer.